PCMCIA Flash Memory Card
2 MEGABYTE through 40 MEGEBYTE (Intel/Sharp based)

FEATURES

- Low cost High Density Linear Flash Card
- Supports 3V or 5V only systems
- x8/ x16 Data Interface
- Based on Intel/Sharp FlashFile Components
- Fast Read Performance
  - 150ns @ 5V
  - 200ns @ 3.3V
- High Performance Random Writes
  - 8µs Typical Word Write Time @ 5V
  - 17µs Typical Word Write Time @ 3.3V
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

GENERAL DESCRIPTION

WEDC's FLV Series Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLV series cards conform to the PCMCIA international standard

The card's control logic provides the system interface and controls the internal Flash memories. The card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLV Flash cards provide removable high-performance disk emulation.

The FLV series offers low power modes controlled by registers. Cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLV series is based on Intel/Sharp Flash memories.

Note: *Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.*

ARCHITECTURE OVERVIEW

WEDC's FLV series is designed to support from 2 to 20 of 8Mb or 16MB components, providing a wide range of density options. Cards are based on the 28F008SC (8Mb) and 28F016SC (16Mb) devices for 3.3V or 5V only applications. Devices codes for the 28F008SC and the 28F016SC are: A6H and AAH respectively. Systems should be able to recognize all the codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments.

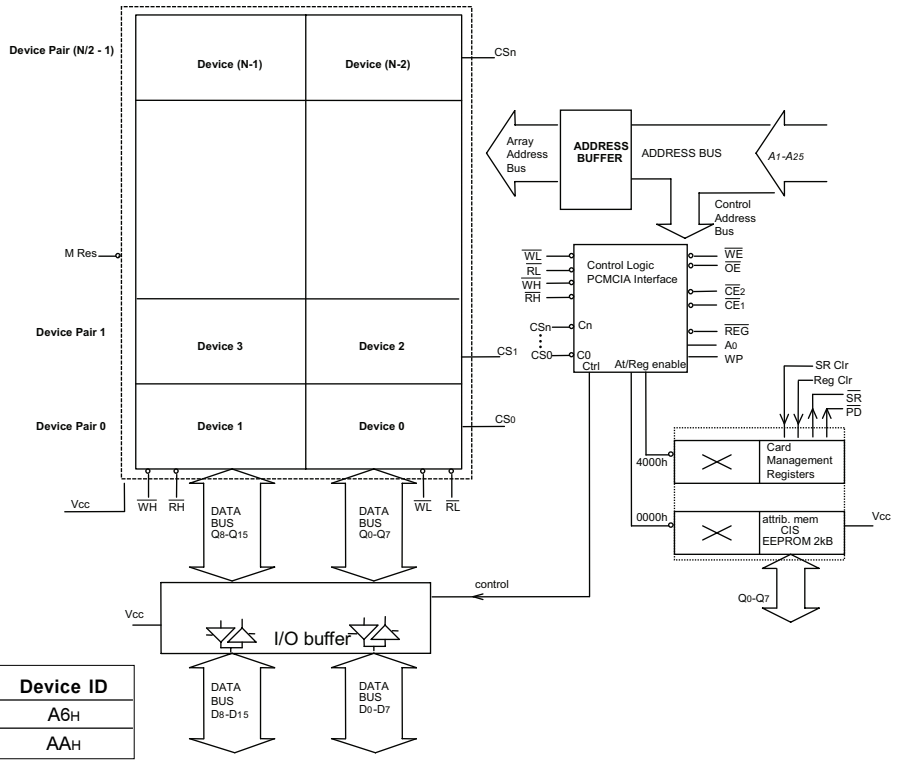
In support of the PC Card 95 standard for word wide access, devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A_0, $\overline{CE_1}$ and $\overline{CE_2}$, 8-bit hosts can access all data on data lines DQ_0 - DQ_7.

The **FLA21-FLA28** series also supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register (cards without attribute memory and versions **FLV51-FLV58** do not have registers). **FLV51-FLV58** do not support Ready/Busy and Reset signals.

The FLV series cards conform to the PC Card (PCMCIA) and JEIDA standards, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.

BLOCK DIAGRAM



Device type	Manuf ID	Device ID
28F008SC	89H	A6H
28F016SC	89H	AAH

REGISTERS IN ATTRIBUTE MEMORY SPACE*

ADDRESS	REGISTER NAME
4100h	Status Register
4002h	Config. and Status Register
4000h	Configuration Option Register

** FLV51- FLV58 and cards without Attribute Memory do not have registers.*

COR

CONFIGURATION OPTION REGISTER: ADRS = 4000h WRITE ONLY

SRES	LREQ	Configuration Index					
D7	D6	D5	D4	D3	D2	D1	D0

D7 Soft Reset, active High
1 = Reset State
0 = End Reset State

D6 Level Req (not supported)

D5-D0 Configuration index (not supported)

CSR

CONFIGURATION STATUS REGISTER: ADRS = 4002h WRITE ONLY

Not Supported					PDwn	Not Supported	
D7	D6	D5	D4	D3	**D2**	D1	D0

D2 Power Down, active High
1 = Place all memory devices in power down mode
0 = Normal Operation Power On default = 0

SR

STATUS REGISTER: ADRS = 4100h READ ONLY

Not Supported		SReset		PDwn	Not Supported		R/BSY
D7	D6	**D5**	D4	**D3**	D2	D1	**D0**

D5 Represents the state of SRESET bit in COR (4000h)
1 = Reset
0 = Normal Operation
Power On default D5 = 0

D3 Represents the state of Power Down bit (D2) in CSR (4002h)
1 = Power Down

D0 Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs. This bit allows software polling of the card's Ready/Busy status.
1 = Ready

PINOUT

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ_3	I/O	Data bit 3	
3	DQ_4	I/O	Data bit 4	
4	DQ_5	I/O	Data bit 5	
5	DQ_6	I/O	Data bit 6	
6	DQ_7	I/O	Data bit 7	
7	$\overline{CE}_1$	I	Card enable 1	LOW
8	A_{10}	I	Address bit 10	
9	$\overline{OE}$	I	Output enable	LOW
10	A_{11}	I	Address bit 11	
11	A_9	I	Address bit 9	
12	A_8	I	Address bit 8	
13	A_{13}	I	Address bit 13	
14	A_{14}	I	Address bit 14	
15	$\overline{WE}$	I	Write Enable	LOW
16	$\overline{RDY/BSY}$	O	Ready/Busy	LOW (4)
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Prog. Voltage	NC
19	A_{16}	I	Address bit 16	
20	A_{15}	I	Address bit 15	
21	A_{12}	I	Address bit 12	
22	A_7	I	Address bit 7	
23	A_6	I	Address bit 6	
24	A_5	I	Address bit 5	
25	A_4	I	Address bit 4	
26	A_3	I	Address bit 3	
27	A_2	I	Address bit 2	
28	A_1	I	Address bit 1	
29	A_0	I	Address bit 0	
30	DQ_0	I/O	Data bit 0	
31	DQ_1	I/O	Data bit 1	
32	DQ_2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	$\overline{CD}_1$	O	Card Detect 1	LOW
37	DQ_{11}	I/O	Data bit 11	
38	DQ_{12}	I/O	Data bit 12	
39	DQ_{13}	I/O	Data bit 13	
40	DQ_{14}	I/O	Data bit 14	
41	DQ_{15}	I	Data bit 15	
42	$\overline{CE}_2$	I	Card Enable 2	LOW
43	VS_1	O	Voltage Sense 1	NC (2)
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address bit 17	
47	A_{18}	I	Address bit 18	
48	A_{19}	I	Address bit 19	
49	A_{20}	I	Address bit 20	
50	A_{21}	I	Address bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Prog. Voltage	NC
53	A_{22}	I	Address bit 22	
54	A_{23}	I	Address bit 23	
55	A_{24}	I	Address bit 24	
56	A_{25}	I	Address bit 25	
57	VS_2	O	Voltage Sense 2	NC
58	$\overline{RST}$	I	Card Reset	HIGH
59	$\overline{Wait}$	O	Extended Bus cycle	Low (3)
60	RFU		Reserved	
61	$\overline{REG}$	I	Attrib Mem Select	
62	BVD_2	O	Bat. Volt. Detect 2	(3)
63	BVD_1	O	Bat. Volt. Detect 1	(3)
64	DQ_8	I/O	Data bit 8	
65	DQ_9	I/O	Data bit 9	
66	DQ_{10}	O	Data bit 10	
67	$\overline{CD}_2$	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

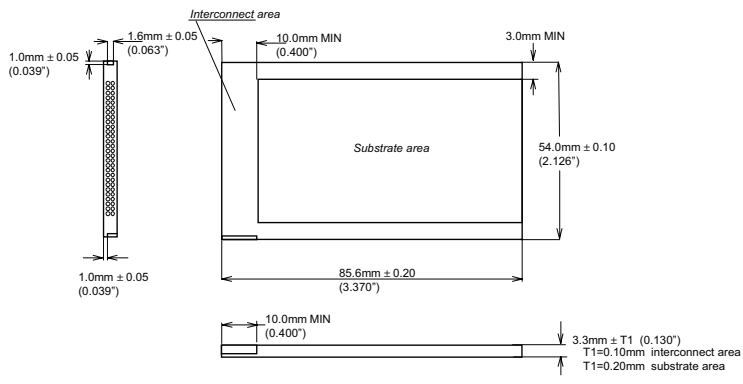
1. $\overline{RDY}$/BSY signal is an "Open drain" type output, pull-up resistor on host side is required.

2. $\overline{Wait}$, BVD_1 and BVD_2 are driven high for compatibility.

3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie: 4MB A_{21} is MSB A_{22}-A_{25} are NC).

*4. NC - No Connection for **FLV51-FLV58***

MECHANICAL



CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64MB of memory on the card. Signal A_0 is not used in word access mode. A_{25} is the most significant bit
DQ_0 - DQ_{15}	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 THROUGH DQ_{15} constitute the bi-directional databus. DQ_{15} is the MSB.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE 1 AND 2:** $\overline{CE}_1$ enables even byte accesses, $\overline{CE}_2$ enables odd byte accesses. Multiplexing A_0, $\overline{CE}_1$ and $\overline{CE}_2$ allows 8-bit hosts to access all data on DQ_0 - DQ_7.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
$\overline{RDY/BSY}$(*)	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
$\overline{CD}_1$, $\overline{CD}_2$	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
V_{PP1}, V_{PP2}	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages for card. Not connected for 3.3V/5V only card.
V_{CC}		**CARD POWER SUPPLY:** 5.0V for all internal circuitry
GND		**CARD GROUND**
$\overline{REG}$	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to attribute memory space, occupied by the Card Information Structure (CIS) and Card Registers.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down control for the memory array.
$\overline{WAIT}$	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are open to indicate a 5V card .
RFU		**RESERVED FOR FUTURE USE**
NC		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

(*) Signals not supported by FLV51-FLV58 (NC)

FUNCTIONAL TRUTH TABLE

READ function						Common Memory			Attribute Memory		
Function Mode	$\overline{CE}_2$	$\overline{CE}_1$	A_0	$\overline{OE}$	$\overline{WE}$	$\overline{REG}$	D_{15}-D_8	D_7-D_0	$\overline{REG}$	D_{15}-D_8	D_7-D_0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

ABSOLUTE MAXIMUM RATINGS (1)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85°C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85°C
Voltage on any pin relative to V_{SS}	-0.5V to V_{CC}+0.5V
V_{CC} supply Voltage relative to V_{SS}	-0.5V to +7.0V

Note:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (1)
V_{CC} = 3.3V/5V

Symbol	Parameter	Density (Mbytes)	Notes	3.3V V_{CC}		5V V_{CC}		Units	Test Conditions
				Typ(3)	Max	Typ(3)	Max		
I_{CCR}	V_{CC} Read Current	All		10	12	20	35	mA	V_{CC} = V_{CC} max tcycle = 150ns, CMOS levels
I_{CCW}	V_{CC} Program Current	All	28F008SC 28F016SC		60		75	mA	
I_{CCE}	V_{CC} Erase Current	All			40		50	mA	
I_{CCS} (CMOS)	V_{CC} Standby Current	2MB	2 28F008SC	50	200	60	230	µA	V_{CC} = V_{CC} max Control Signals = V_{CC} Reset = V_{SS}, CMOS levels
		20MB		400		420			
		4MB	2 28F016SC	50	200	60	230		
		40MB		400		420			

CMOS Test Conditions: V_{CC} = 5V ± 5%, V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V

Notes:
1. *All currents are RMS values unless otherwise specified. I_{CCR}, I_{CCW} and I_{CCE} are based on Byte wide operations. For 16 bit operation values are double.*
2. *Control Signals: $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$, $\overline{WE}$, $\overline{REG}$.*
3. *Typical: V_{CC} = 5V, T = +25°C.*

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX V_{IN} =V_{CC} or V_{SS}
I_{LO}	Output Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX V_{OUT} =V_{CC} or V_{SS}
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7xV_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	1	V_{CC}-0.4	V_{CC}	V	I_{OH} = -2.0mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	2.0		V	

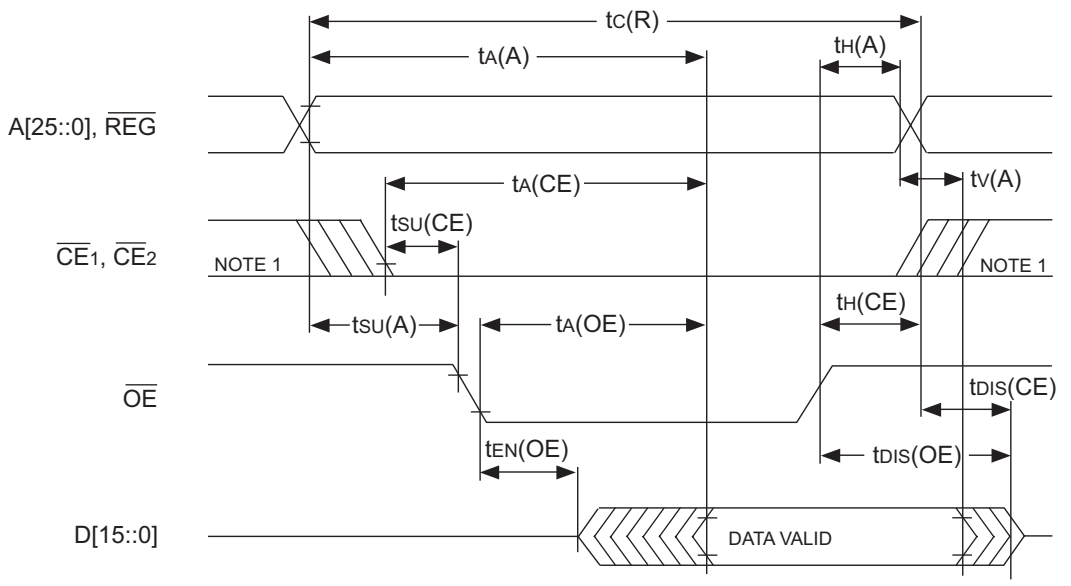
Notes:
1. *Values are the same for byte and word wide modes for all card densities.*
2. *Exceptions: Leakage currents on $\overline{CE_1}$, $\overline{CE_2}$, $\overline{OE}$, $\overline{REG}$ and $\overline{WE}$ will be < 500 µA when V_{IN} = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when V_{IN}=V_{CC} due to internal pull-down resistor.*

AC CHARACTERISTICS - READ TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	150ns		250ns		Unit
		Min	Max	Min	Max	
$t_{C}(R)$	Read Cycle Time	150		250		ns
$t_{A}(A)$	Address Access Time		150		250	ns
$t_{A}(CE)$	Card Enable Access Time		150		250	ns
$t_{A}(OE)$	Output Enable Access Time		75		125	ns
$t_{SU}(A)$	Address Setup Time		20		30	ns
$t_{SU}(CE)$	Card Enable Setup Time		0		0	ns
$t_{H}(A)$	Address Hold Time		20		30	ns
$t_{H}(CE)$	Card Enable Hold Time		20		30	ns
$t_{V}(A)$	Output Hold from Address Change		0		0	ns
$t_{DIS}(CE)$	Output Disable Time from $\overline{CE}$		75		100	ns
$t_{DIS}(OE)$	Output Disable Time from $\overline{OE}$		75		100	ns
$t_{EN}(CE)$	Output Enable Time from $\overline{CE}$	5		5		ns
$t_{EN}(OE)$	Output Enable Time from $\overline{OE}$	5		5		ns
$t_{REC}(RSR)$	Power Down recovery to Output Delay. V_{CC} = 5V		500		600	ns

Note: *AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.*

READ TIMING DIAGRAM



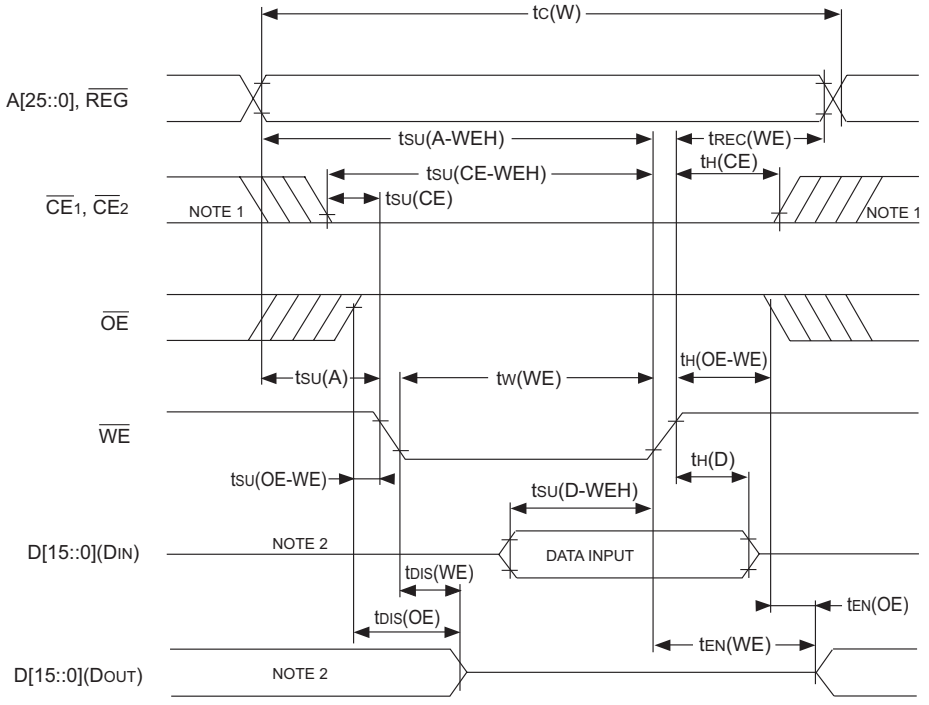
Note: *Signal may be high or low in this area.*

AC CHARACTERISTICS - WRITE TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
tcW	Write Cycle Time	150		250		ns
tw(WE)	Write Pulse Width	80		150		ns
tsu(A)	Address Setup Time	20		30		ns
tsu(A-WEH)	Address Setup Time for $\overline{WE}$	100		180		ns
tsu(CE-WEH)	Card Enable Setup Time for $\overline{WE}$	100		180		ns
tsu(D-WEH)	Data Setup Time for $\overline{WE}$	50		80		ns
tH(D)	Data Hold Time	20		30		ns
tREC(WE)	Write Recover Time	20		30		ns
tDIS(WE)	Output Disable Time from $\overline{WE}$		75		100	ns
tDIS(OE)	Output Disable Time from $\overline{OE}$		75		100	ns
tEN(WE)	Output Enable Time from $\overline{WE}$	5		5		ns
tEN(OE)	Output Enable Time from $\overline{OE}$	5		5		ns
tsu(OE-WE)	Output Enable Setup from $\overline{WE}$	10		10		ns
tH(OE-WE)	Output Enable Hold from $\overline{WE}$	10		10		ns
tsu(CE)	Card Enable Setup Time from $\overline{OE}$	0		0		ns
tH(CE)	Card Enable Hold Time	20		20		ns

Note: *AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.*

WRITE TIMING DIAGRAM



Notes:

1. Signal may be high or low in this area.

2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D_{15} - D_0) by the host system.

DATA WRITE AND ERASE PERFORMANCE (1,3)

V_{CC} = 5V ± 5%, T_A = 0C° TO + 70C°

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	4		8		µs
t_{WHQV2} t_{EHQV2}	Block Program Time	Device SC	0.4	0.5		sec
	Block Erase Time	Device SC	0.9	1.1		sec

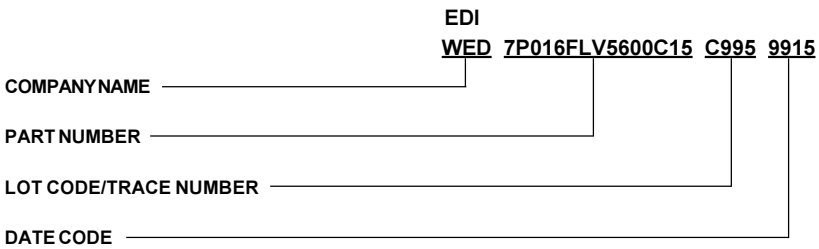
V_{CC} = 3.3V ± 0.3V, T_A = 0C° TO + 70C°

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	4		17		µs
t_{WHQV2} t_{EHQV2}	Block Program Time	Device SC	0.4	1.1		sec
	Block Erase Time	Device SC	0.9	1.8		sec

Notes:

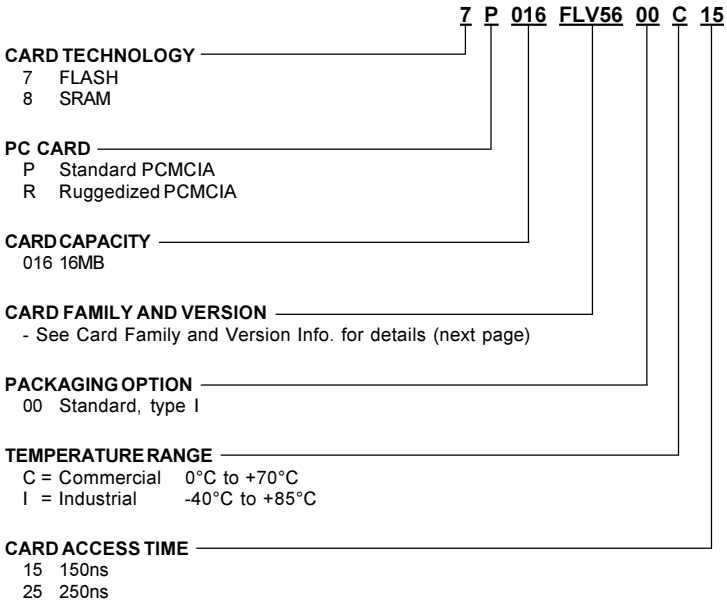
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance $\overline{RDY/BSY}$ signal should be polled.

PRODUCT MARKING



Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING



CARD FAMILY AND VERSION INFORMATION

FLV21-FLV24 Based on **28F008SC** for 3.3V/5V application

FLV21 No Attribute Memory, no Write Protect switch
FLV22 With Attribute Memory, no Write Protect switch
FLV23 No Attribute Memory, with Write Protect switch
FLV24 With Attribute Memory, with Write Protect switch
Example P/N **7P XXX FLV 22 SS T ZZ**

FLV25-FLV28 Based on **28F016SC** for 3.3V/5V application

FLA25 No Attribute Memory, no Write Protect switch
FLA26 With Attribute Memory, no Write Protect switch
FLA27 No Attribute Memory, with Write Protect switch
FLA28 With Attribute Memory, with Write Protect switch
Example P/N **7P XXX FLV 26 SS T ZZ**

FLV51-FLV54 Based on **28F008SC** for 3.3V/5V application. The same as FLA21-FLA24 with exception:

- no registers
- signals RST, RDY/BSY, Wait are not connected

FLA51 No Attribute Memory, no Write Protect switch
FLA52 With Attribute Memory, no Write Protect switch
FLA53 No Attribute Memory, with Write Protect switch
FLA54 With Attribute Memory, with Write Protect switch
Example P/N **7P XXX FLV 52 SS T ZZ**

FLV55-FLV58 Based on **28F016SC** for 3.3V/5V application. The same as FLA25-FLA28 with exception:

- no registers
- signals RST, RDY/BSY, Wait are not connected

FLA55 No Attribute Memory, no Write Protect switch
FLA56 With Attribute Memory, no Write Protect switch
FLA57 No Attribute Memory, with Write Protect switch
FLA58 With Attribute Memory, with Write Protect switch
Example P/N **7P XXX FLV 56 SS T ZZ**

ORDERING INFORMATION

7P XXX FLVYY SS T ZZ

XXX

002[1]	2MB	012	12MB	024[2]	24MB
004	4MB	014[1]	14MB	028[2]	28MB
006[1]	6MB	016	16MB	032[2]	32MB
008	8MB	018[1]	18MB	036[2]	36MB
010[1]	10MB	020	20MB	040[2]	40MB

[1] available only for FLV21/51–FLV24/54

[2] available only for FLV25/55–FLV28/58

FLVYY

Card Version (See card family and version information)

SS

00	WEDC Silkscreen
01	Blank Housing, Type I
02	Blank Housing, Type I Recessed

T

C	Commercial
I**	Industrial

ZZ

15	150ns

***Denotes advanced information.*

ADDRESS	VALUE	DESCRIPTION
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	FLASH = 150ns (device writable)
06H	**0EH**	CARD SIZE: 4MB
	1EH	8MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	**FFH**	END OF DEVICE
0AH	**1CH**	**CISTPL_DEVICE_OC**
0CH	**04H**	TPL_LINK
0EH	**02H**	3 VOLT OPERATION
10H	**51H**	FLASH = 250ns (device writable)

ADDRESS	VALUE	DESCRIPTION
12H	**0EH**	CARD SIZE: 4MB
	1EH	4MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
14H	**FFH**	END OF DEVICE
16H	**18H**	**CISTPL_JEDEC_C**
18H	**03H**	TPL_LINK
1AH	**89H**	INTEL - ID
1CH	**AAH**	INTEL 28F016SC – ID(4-40MB)
1EH	**FFH**	END OF DEVICE
20H	**17H**	**CISTPL_DEVICE_A**
22H	**03H**	TPL_LINK

CIS Information for FLV Series Cards

Example for FLV26 family, 4MB, built with 28F016SC

ADDRESS	VALUE	DESCRIPTION
24H	42H	EEPROM - 200ns
26H	01H	Device Size = 2KBytes
28H	FFH	END OF TUPLE
2AH	1DH	CISTPL_DEVICE_OA
2CH	03H	TPL_LINK
2EH	02H	3 VOLT OPERATION
30H	11H	ROM - 250ns
32H	FFH	END OF DEVICE
34H	1AH	CISTPL_CONF
36H	06H	TPL_LINK
38H	01H	TPCC_SZ
3AH	00H	TPCC_LAST
3CH	00H	TPCC_RADR
3EH	40H	TPCC_RADR
40H	03H	TPCC_RMSK
42H	FFH	CISTPL_END
44H	1EH	CISTPL_DEVICEGEO
46H	06H	TPL_LINK
48H	02H	DGTPL_BUS
4AH	11H	DGTPL_EBS
4CH	01H	DGTPL_RBS
4EH	01H	DGTPL_WBS
50H	01H	DGTPL_PART
52H	01H	FLASH DEVICE NON-INTERLEAVED
54H	20H	CISTPL_MANFID
56H	04H	TPL_LINK(04H)
58H	F6H	EDI TPLMID_MANF: LSB
5AH	01H	EDI TPLMID_MANF: MSB
5CH	00H	*LSB: Number Not Assigned*
5EH	00H	*MSB: Number Not Assigned*
60H	15H	CISTPL_VERS1
62H	47H	TPL_LINK
64H	05H	TPLLV1_MAJOR
66H	00H	TPLLV1_MINOR
68H	45H	*E*
6AH	44H	*D*
6CH	49H	*I*
6EH	37H	*7*
70H	50H	*P*
72H	30H	*0*
74H	34H	*4*
76H	30H	*0*
78H	46H	*F*
7AH	4CH	*L*
7CH	56H	*V*
7EH	32H	*2*
80H	36H	*6*
82H	2DH	*-*
84H	2DH	*-*
86H	2DH	*-*
88H	31H	*1*

ADDRESS	VALUE	DESCRIPTION
8AH	35H	*5*
8CH	20H	SPACE
8EH	00H	END TEXT
90H	43H	*C*
92H	4FH	*O*
94H	50H	*P*
96H	59H	*Y*
98H	52H	*R*
9AH	49H	*I*
9CH	47H	*G*
9EH	48H	*H*
A0H	54H	*T*
A2H	20H	SPACE
A4H	45H	*E*
A6H	4CH	*L*
A8H	45H	*E*
AAH	43H	*C*
ACH	54H	*T*
AEH	52H	*R*
B0H	4FH	*O*
B2H	4EH	*N*
B4H	49H	*I*
B6H	43H	*C*
B8H	20H	SPACE
BAH	44H	*D*
BCH	45H	*E*
BEH	53H	*S*
C0H	49H	*I*
C2H	47H	*G*
C4H	4EH	*N*
C6H	53H	*S*
C8H	20H	SPACE
CAH	49H	*I*
CCH	4EH	*N*
CEH	43H	*C*
D0H	4FH	*O*
D2H	52H	*R*
D4H	50H	*P*
D6H	4FH	*O*
D8H	52H	*R*
DAH	41H	*A*
DCH	54H	*T*
DEH	45H	*E*
E0H	44H	*D*
E2H	20H	SPACE
E4H	00H	END TEXT
E6H	31H	*1*
E8H	39H	*9*
EAH	39H	*9*
ECH	37H	*7*
EEH	00H	END TEXT
F0H	FFH	END OF LIST

Document Title

PCMCIA Flash Memory Card - FLV Series

Revision History

Rev level	Description	Date
Rev 0	Initial release	September, 1998
Rev 1	CIS, value in line 0CH	December 2, 1998
Rev 2	Logo change	June 7, 1999
Rev 3	Added page 9, revised page 10, changed page header	May 30, 2000
Rev 4	Final release	
Rev 5	FLV51-58 added, removed support for 4Mb components	March 17, 2003